REMARKS

Applicants respectfully request reconsideration of this application as amended. Claims 1, 6, 14, 25, 28, and 31 have been amended without prejudice. Claims 32-35 have been cancelled without prejudice. No claims have been added. Therefore, claims 1, 6, 14, and 23-31 are presented for examination.

35 U.S.C. § 101 Rejection

Claims 24, 27, 30 and 34 are rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility. The undersigned disagrees with the Examiner's characterization of a bus. However, to expedite prosecution of the present application the independent claims have been amended making the Examiner's rejection moot.

35 U.S.C. § 112 Rejection

Claims 5, 9, 13 and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Again, the undersigned disagrees with the Examiner's characterization of a bus. This rejection, however, is moot in light of the current amendments.

Claims 32-35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Claims 32-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. Claims 32-35 have been cancelled without prejudice.

Claims 1, 6, 14, and 23-35 are rejected 35 U.S.C. 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention. Applicants submit that the current amendments overcome this rejection.

35 U.S.C. § 102 Rejection

Claims 1, 6, 14 and 23-35 are rejected under 35 U.S.C. §102(e) as being anticipated by Dabral, et al., U.S. Patent No. 6,601,196 ("Dabral").

Claim 1, as amended, recites:

> an observability buffer having a trigger, wherein the observability buffer is integrated on a first component which is capable of being communicably coupled with a second component via a simultaneous bi-directional (SBD) interface having ternary logic levels, wherein the observability buffer is configured to un-intrusively observe and echo one or more of a plurality of signals transmitted between the first component and the second component based on one or more of a control signal-based indication, an address signal-based indication, and a time-based indication; and
> an observability port on the first component capable of receiving the echoed signals from the observability buffer and providing a diagnostic device access to the echoed signals.
> (emphasis provided)

As presently understood by Applicants, Dabral generally relates to an apparatus and method for debugging a bus including ***interposing a device*** that monitors the data transferred between two devices on the bus (see Abstract). In contrast, claim 1, in pertinent part, expressly recites that "the observability buffer is integrated on a first component" (emphasis provided). Applicants can find no disclosure, teaching, or reasonable suggestion in Dabral of the observability buffer being integrated on a component.

On page 3 of a previous Office action that was mailed May 3, 2005, the Examiner suggests that Figure 2 Number 250, Column 1 Lines 12-14 and Column 3 Lines 15-18 teach "a buffer having a trigger integrated on a component with a simultaneous bi-

directional (SBD) memory bus having ternary logic levels." However, the sections of Dabral cited by the Examiner do not teach or reasonably suggest that the observability buffer is integrated on the device. In particular, Figure 2 shows that the device is ***interposed*** between the two devices. For example, column 1 lines 12-14 and column 3 lines 15-18 of Dabral recite:

> Computer systems commonly make use of busses to transfer data between devices that include processors, storage devices and I/O devices. Many of such busses make use of one or more data lines, which are electrical conductors on which signals are used to transfer data in concert with a clock signal and/or one or more control signals.
>
> In one embodiment, busses 200a and 200b are ternary logic busses that enable the substantially simultaneous bidirectional transfer of data to and from each of devices 210 and 212.

Accordingly, Applicants respectfully request the withdrawal of the rejection of claim 1 and its dependent claims.

Claims 6 and 14 contain limitations similar to those of claim 1. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 6 and 14 and their dependent claims.

Conclusion

In light of the foregoing, reconsideration and allowance of the claims is hereby earnestly requested.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

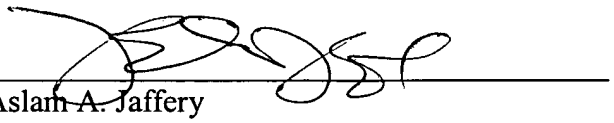
Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: June 22, 2006



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